UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,168	10/30/2001	Makoto Ono	16869P-037300US	8661

20350 7590 04/01/2003

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 04/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/004,168	Applicant(s) ONO ET AL.	
	Examiner Stacy A Whitmore	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,27,28,31 and 36-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,27,28,31 and 36-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Applicant's election without traverse of Group I, claims 21, 27-28, 31, and 36-38 in Paper No. 6 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 21, 27, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atchison (US Patent 6,324,481) in view of Kircsh (US Patent 6,507,933).

3. As for claim 21, Atchison disclosed the invention substantially as claimed, including an inspection system comprising

an inspection apparatus for detecting positions and sizes of particles or pattern defects on an object to be inspected [col. 4, lines 46-55];

an image taking apparatus for taking images of said particles or said pattern defects as detected by said inspection apparatus [col. 1, line 63 col. 2, line 15 and figure 7 elements 132, 134, and 136; col. 4, lines 46-55];

an analysis unit operatively coupled to said inspection apparatus and said image taking apparatus, said analysis unit including [col. 1, line 63 col. 2, line 15 and figure 7 elements 132, 134, and 136]; col. :

a storage device for storing therein inspection data produced by said inspection apparatus and position information of regions of a circuit pattern to be formed on said object [col. 4, line 46 –col. 5, line 19, especially col. 5, lines 9-10 for the storage device];

a calculation device for identifying particle and pattern defects that are correspondingly positioned in said regions, and calculating failure probabilities for said particles and said pattern defects positioned in said regions based on their sizes [col. 4, line 46 –col. 6, line 20, especially col.'s 5-6, where the specific calculations are done]; and

a selection device for selecting particles or pattern defects for calculated failure probabilities [col. 4, line 46 –col. 6, line 20, especially col.'s 5-6, where defects of interest and defect types are disclosed].

Atchison did not specifically disclose selecting particles or pattern defects whose calculated failure probabilities are greater than or equal to a predetermined threshold.

Kirsch disclosed selecting defects where failure probabilities are equal to or greater than a predetermined threshold [col. 4, lines 56-67].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Atchison and Kirsch because selecting particles or pattern defects equal to or greater than a predetermined threshold value in Atchison's system would have allowed for Atchison's system to set quality control limits on defects to set acceptable limits within desired limits which would improve the production process [see Kirsch col. 4, lines 56-67].

4. As for claim 36, Atchison disclosed the invention substantially as claimed, including a method for manufacturing semiconductor devices comprising the steps of:

a fabrication step for forming circuit patterns on or over a wafer, said circuit patterns constituting a plurality of semiconductor chips [col.'s 1-2];

an inspection step for detecting positions and sizes of particles or pattern defects on an said wafer [col.'s 4-5];

identifying positions and sizes of those of said particles or said pattern defects located in a region of said circuit patterns that constitute one of said semiconductor chips [col.'s4-5];

a calculation step for calculating failure probabilities based on sizes of said pattern defects in said region [col. 4, line 46 –col. 6, line 20, especially col.'s 5-6, where the specific calculations are done];

an extraction step for extracting positions of said particles or said pattern defects with calculated failure probabilities [col. 4, line 64 – col. 5, line 29]; and

producing images of said particles or said pattern defects extracted at said extraction step [col. 4, line 64 – col. 5, line 29, especially col. 5, lines 14-17].

Atchison did not specifically disclose that positions of particles or defects are extracted for a calculated failure probability greater than or equal to a predefined threshold. Kirsch disclosed an equal to or greater than threshold for extracting wafers with defects [col. 4, lines 56-67].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Atchison and Kirsch because extracting particles or pattern defects equal to or greater than a predetermined threshold value in Atchison's system would have allowed for Atchison's system to set quality control limits on defects to set acceptable limits within desired limits which would improve the production process [see Kirsch col. 4, lines 56-67].

5. As for claim 27, Atchison disclosed a simulation device for generating virtual defects at random positions with respect to circuit graphics obtainable from mask layout data forming said circuit pattern, and computing said failure probabilities from connection relationships of said circuit graphics and said defects [col. 5, lines 1-15, and 57-67; and col. 6, lines 1-7].

6. Claims 24, 28, 31, and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atchison (US Patent 6,324,481) in view of Kircsh (US Patent 6,507,933).

As for claims 24, 28, 31, and 37-38, Atchison in view of Kirsch disclosed the invention substantially as claimed, including the method and apparatus for inspecting semiconductor devices as cited in the rejections of claims 21, 27-28, and 36 above, and further disclosed said position information of said regions is generated from mask layout data of circuit blocks, and [see Atchison, as cited in the rejection of claims 21, and 36].

Atchison in view of Kirsch did not specifically disclose circuit blocks are formed as LSI chip and include memory and logic portions.

Hashimoto disclosed system LSI with logic and memory portions and mask layout data [col. 3, lines 50-54; and col. 9, lines 50-60].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Atchison in view of Kirsch and Hashimoto because Atchison in view of Kirsch disclosed the inspection system and method including semiconductor IC's [see Atchison, col. 1, lines 35-45] which comprise integrated circuits such as LSI's, and Hashimoto disclosed system LSI's including logic and memory portions. The inspection of circuit blocks within system LSI's and the position information of said regions which is generated from mask layout data of circuit blocks would have allowed Atchison in view of Kirsch's inspection system to evaluate defect conditions of well known circuits such as the LSI for the manufacturing of good circuits with as little defect as possible.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703)

305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore
Patent Examiner
Art Unit 2812

SAW
March 27, 2003